IN THE CLAIMS

Following is a complete set of claims as amended with this response, which includes an amendment to claim 3.

1. (canceled)

2. (previously amended) The method of claim 3, further comprising selecting said memory banks for access by one of the first and second processors.

3. (currently amended) A method for allocating real-time audio data from a plurality of audio channels in a system having a first processor and a second processor, the method comprising:

providing a plurality of memory banks of semiconductor memory devices, each memory bank being accessible to the first and second processors for operations selected from the group comprising read and write operations, the ~~second~~ plurality of memory banks includes two memory banks; and

storing subsets of said audio data in the ~~second~~ plurality of memory banks, the subsets corresponding to different groups of audio channels.

4. (original)The method of claim 3 wherein one subset of said audio data corresponds to even-numbered audio channels and one other subset of said audio data corresponds to odd-numbered audio channels.

5. (canceled)

6. (previously amended) A system having first and second buses for processing real-time audio data from a plurality of audio channels, the system comprising:

a first processor and a second processor coupled to said first and second busses, respectively;

a plurality of memory banks of semiconductor memory devices coupled to said first and second buses for storing said audio data, said plurality of memory banks being accessible to the

first and second processors for operations selected from the group comprising read and write operations, said plurality of memory banks storing subsets of audio data, said subsets corresponding to different groups of audio channels; and

a plurality of selectors coupled said first and second buses to select said memory banks for access by one of said first and second processors.

7. (previously amended) The system of claim 6 wherein the plurality of selectors include a plurality of address multiplexers and data transceivers.

8. (previously amended) The system of claim 6 wherein one subset of said audio data corresponds to even-numbered audio channels and one other subset of said audio data corresponds to odd-numbered audio channels.

9. (previously amended) The system of claim 6, wherein the memory banks include dynamic random access memories.

10. (previously amended) The method of claim 3, wherein storing further comprises interleaving the subsets of data.

11. (previously amended) The system of claim 6, wherein the subsets are stored in the memory banks in an interleaving manner.

12. (previously amended) The method of claim 3, wherein storing comprises storing one of the subsets of audio data in one of the memory banks, said method further comprising reading stored audio data from a second of the memory banks.

13. (previously amended) The method of claim 3, wherein the first processor performs a read operation on a first memory bank of the plurality of memory banks and the second processor performs a write operation on a second memory bank of the plurality of memory banks.

14. (previously amended) The system of claim 6, wherein subsets of audio data are stored in one of the memory banks and stored audio data is read from a second memory bank of the memory banks.

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15. (previously amended) The system of claim 6, wherein the first processor performs a read operation on a first memory bank of the plurality of memory banks and the second processor performs a write operation on a second memory bank of the plurality of memory banks.